Remarks

Applicant notes with appreciation the indication that Claims 11-26 and 31-42 are allowed, and that Claims 2 and 9-10 are directed toward allowable subject matter. Reconsideration of the above referenced application in view of the enclosed remarks is requested. Claims 1-8 are amended. Specifically, Claim 2 is amended to put it into independent form. Claims 1-42 are now pending in the application.

ARGUMENT

Claims 1, 3-8, 27, and 29-30 are rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Pat. No. 6,807,595 to Khan et al. (hereinafter "Khan et al."). This rejection is respectfully traversed and Claims 3-8 and 28-30 are believed allowable based on the following discussion.

Regarding Claim 1, the Examiner asserts that Khan et al. teach determining whether the device is activated or inactivated. Applicant's claim requires *determining whether the file system device is activated or inactivated*. In contrast, Khan et al. teach only to determine whether the microprocessor is activated or inactivated. Applicant's claimed invention is meant to buffer requests to write to a *file system device* to reduce power consumption of unnecessarily activating the file system device. In contrast, Khan et al. teach buffering interrupt requests when a microprocessor is inactivated. Khan et al. do not teach or suggest anything related to a file system device. The device of Khan et al. is a microprocessor. Applying the teaching of Khan et al. will not result in Applicant's invention.

Similarly, Claim 27 requires *determining a power state of a non-volatile storage device*. In contrast, Khan et al. teach determining that a microprocessor is activated or inactivated. Khan et al. do not teach a power state of a non-volatile storage device. In known computer systems, a microprocessor is typically a separate device than the non-volatile storage device. The microprocessor may communicate with the storage device, but knowing the power state of the microprocessor does not determine the power state of the storage device. Thus, Claims 1 and 27 and their progeny are believed allowable, as amended.

Claim 2 has been amended to put it into independent form. Claims 3-6 are now dependent on allowable Claim 2 and are therefore believed to be allowable.

Claims 7 is amended to put it into independent form. Claim 7 requires that the predetermined condition comprises one or more of the following: detecting that a memory write buffer is full, detecting that a predetermined amount of time has lapsed, detecting that a predetermined volume of data has been buffered, detecting that battery power is at a threshold level, detecting that a computer system with which the device is associated is being turned off or put in a standby state, and detecting an explicit request that the write buffer contents be committed to non-volatile storage. The Examiner asserts that this limitation is taught by Khan et al at Col. 7, lines 9-21.

Khan et al. teach that an interrupt controller, upon receiving an interrupt request,

"determines whether the microprocessor is in a power shut down mode and, if so, whether the interrupt request is of sufficient priority to justify powering up the microprocessor. If so, the interrupt controller forwards appropriate signals to the microprocessor for powering up the microprocessor so that the microprocessor can process and respond the interrupt request. If not, the interrupt controller merely stores the interrupt request pending a subsequent power up operation by the microprocessor." [emphasis added]

Khan et al. do not teach that a *predetermined amount of time* is detected, which comprises a predetermined condition. Khan et al. teach merely that the interrupt controller determines whether the microprocessor is currently in power shutdown mode. Further, Khan et al. do not teach or suggest *detecting that a computer system is being turned off or put in standby state*. Khan et al. teach merely determining that the microprocessor is already in a power shut down mode. Khan et al. do not teach or suggest determining a *change in state or mode*, which is recited in the claimed invention. Applicant's claimed invention requires that the change in state is the predetermined condition, i.e., detecting that the computer system is *being* turned off or *being* put into standby mode. Khan et al. only teach detecting that the microprocessor is already in a power shut down state.

Thus, applying Khan et al. to Applicant's invention will not result in a system that will be capable of writing contents of the buffer to non-volatile storage when detecting a change in

power state. Applicant's claimed invention is capable of detecting when the computer system is about to be put into sleep mode or shut down, which enables buffered information to be written before the computer system mode has changed. In contrast, Khan et al. will only enable a microprocessor to buffer requests when the microprocessor is already shut down.

Regarding Claim 8, Applicant's claimed invention requires that a user input requests that the buffered write is to be committed to non-volatile storage. In response to the request, any buffered writes are committed to the appropriate device. Khan et al. do not teach or suggest that a user can explicitly request that buffered information be written to a device. Instead, Khan et al. teach that a keyboard entry must be read in response to an interrupt request. Thus, Claims 7 and 8 are believed allowable.

As for Claim 30, the Examiner asserts that Khan et al. teach information for causing a machine to deactivate the device after writing one or more buffered write operations. Firstly, Khan et al. do not teach or suggest altering the power mode for a non-volatile storage device, but only to activate and restore context to a microprocessor. Khan et al. teach merely storing or buffering interrupt service requests. Secondly, upon completion of the interrupt service routine (ISR) the microprocessor is restored to its previous context. At no time to Khan et al. teach or suggest that a non-volatile storage device should be deactivated after writing buffered write operations. Restoring a context of the microprocessor, as taught by Khan et al. will not result in the deactivation of a non-volatile storage device, as recited in Applicant's claim. Thus, Claim 30 is believed allowable.

Claim 28 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Khan et al. in view of U.S. Pat. No. 6,412,045 to DeKoning et al. (hereinafter "DeKoning et al."). This rejection is respectfully traversed and Claim 28 is believed allowable based on the foregoing and following discussion.

Applicant has discussed the teachings of DeKoning et al. in the previous response, and reinstates these arguments. Specifically, DeKoning et al. teach determining whether cache batteries are operational, i.e., whether caching may take place without fear of data loss, but do not teach determining a power state of a non-volatile storage device. DeKoning et al. merely teach whether an operational battery is present. In addition, as discussed above, Khan et al. do not teach or suggest buffering a write request, but only interrupt requests. Thus, combining the

teachings of Khan et al. with DeKoning et al. will not result in Applicant's claimed invention. All claims remaining in the application are now allowable.

CONCLUSION

In view of the foregoing, Claims 1 to 42 are all in condition for allowance. If the Examiner has any questions, the Examiner is invited to contact the undersigned at (703) 633-6845. Early issuance of Notice of Allowance is respectfully requested. Please charge any shortage of fees in connection with the filing of this paper, including extension of time fees, to Deposit Account 02-2666 and please credit any excess fees to such account.

Respectfully submitted,

Dated: May 17, 2005 *s/ Joni D. Stutman-Horn /*

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